produce addresses 0 and 16. These are written (WR) to the addresses 0 and 8 of the fast buffer memory SRAM. With a delay which is required for partly filling the memory, the data are read page-for-page in linear fashion, that is to say, in table 1, under SRAM (RD) the addresses 0-3, then 8-11 etc. The content of these SRAM addresses is written page-for-page in linear fashion to the appropriate addresses, which are conditional on the transform, of the slow page-oriented memory (column DRAM (WR)), that is to say on the basis of 0-3, 16-19, 4-7 etc., in the example. The use of the small fast memory therefore optimizes access to the page-oriented memory DRAM such that the slow page changes required are as few as possible.

The transforms and memory sizes mentioned above and explained serve only as an illustration. In practice, the slow memory is much larger than the fast memory. By way of example, the slow memory is normally designed for N = 8192, with the slow memory having a page size of P = 16. The small memory therefore has a size of 64 addresses. In an integrated implementation, the fast small memory is therefore of barely any consequence in terms of surface area, but calculation of the FFT or IFFT or of similar discrete orthogonal transforms is significantly speeded up on account of the minimization of the page changes in the slow memory.

List of reference numerals

1 Page-oriented memory
2 Butterfly
3 Page-oriented memory
4 Page-oriented memory
5 Fast memory